

WHAT IS CLAIMED IS:

1 1. A method for processing integrated circuit devices, the method
2 comprising:
3 providing a monitor wafer, the monitor wafer comprising a silicon material;
4 introducing a plurality of particles within a depth of the silicon material,
5 whereupon the plurality of particles have a reduced activation energy within the silicon
6 material;
7 subjecting the monitor wafer including the plurality of particles into a rapid
8 thermal anneal process;
9 applying the rapid thermal anneal process at a first state including a first
10 temperature, the first temperature being within a range defined as a low temperature range,
11 the low temperature range being less than 650 Degrees Celsius;
12 removing the monitor wafer;
13 measuring a sheet resistivity of the monitor wafer;
14 determining the first temperature within a tolerance of less than 2 percent
15 across the monitor wafer; and
16 operating the rapid thermal process using a plurality of production wafers if
17 the first temperature is within a tolerance of a specification temperature.

1 2. The method of claim 1 wherein the introducing of particles
2 comprising:
3 implanting silicon bearing impurities into the silicon material to cause the
4 silicon material to be in an amorphous state; and
5 implanting boron bearing impurities into the silicon material, whereupon the
6 boron bearing impurities are free from activation as applied to the silicon material.

1 3. The method of claim 2 wherein the silicon bearing impurities are
2 implanted using a dose of 1×10^{14} atoms/cm².

1 4. The method of claim 2 wherein the boron bearing impurities are
2 implanted using a dose of 3.5×10^{15} atoms/cm².

1 5. The method of claim 1 wherein the first temperature is less than 650
2 Degrees Celsius.

1 6. The method of claim 1 wherein the first temperature is less than 550
2 Degrees Celsius.

1 7. The method of claim 1 wherein the silicon material is in an amorphous
2 state upon deposition.

1 8. The method of claim 1 wherein the sheet resistivity is provided in a
2 separate tool.

1 9. The method of claim 1 wherein the operating of the production wafers
2 occurs for 24 hours.

1 10. The method of claim 1 wherein the monitor wafer is characterized by a
2 temperature sensitivity of at least 1 Ohms per Degree Celsius.

1 11. A method for processing integrated circuit devices, the method
2 comprising:

3 providing a monitor wafer, the monitor wafer comprising a silicon material
4 having a thickness to a predetermined depth;

5 implanting silicon bearing impurities into the silicon material to cause the
6 silicon material to be in an amorphous state within a portion of the thickness of the silicon
7 material;

8 implanting boron bearing impurities into the silicon material within at least the
9 portion of thickness in the amorphous state, whereupon the boron bearing impurities are free
10 from activation as applied to the silicon material and have a reduced activation energy within
11 the silicon material;

12 subjecting the monitor wafer including the silicon bearing impurities and
13 boron bearing impurities into a rapid thermal anneal process;

14 applying the rapid thermal anneal process at a first state including a first
15 temperature to activate a portion of the boron bearing impurities, the first temperature being
16 within a range defined as a low temperature range, the low temperature range being less than
17 650 Degrees Celsius;

18 removing the monitor wafer;

19 measuring a sheet resistivity of the monitor wafer;

20 determining the first temperature within a tolerance of less than 2 percent
21 across the monitor wafer; and

22 operating the rapid thermal process using a plurality of production wafers if
23 the first temperature is within a tolerance of a specification temperature.

1 12. The method of claim 11 wherein the activated boron bearing impurities
2 influence the sheet resistivity.

1 13. The method of claim 11 wherein the monitor wafer comprising the
2 boron bearing impurities and the silicon bearing impurities are characterized by a temperature
3 sensitivity of at least 1 Ohms per Degree Celsius.

1 14. The method of claim 11 wherein the range being less than 550 Degrees
2 Celsius.

1 15. The method of claim 11 wherein the silicon bearing impurities are
2 implanted using a dose of 1×10^{14} atoms/cm².

1 16. The method of claim 11 wherein the boron bearing impurities are
2 implanted using a dose of 3.5×10^{15} atoms/cm².

1 17. The method of claim 11 wherein the tolerance of the temperature
2 specification is less than 1 percent across the monitor wafer.

1 18. The method of claim 11 wherein the plurality of production wafers is
2 at least 100 wafers.

1 19. The method of claim 11 wherein the monitor wafer is a silicon wafer.

1 20. The method of claim 11 further comprising storing the monitor wafer
2 after the boron implanting and silicon implanting.